New Module Structure Using Flip-Chip Technology for High-Speed Optical Communication ICs

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Abstract

This paper describes a new module structure for 40-Gbit/s class ICs. This structure can eliminate cavity resonance in the package and excitation of parasitic propagation modes in RF feedthroughs. Additionally, the design makes use of flip-chip technology to minimize the parasitic reactance that can occur at interconnections between chips and substrates. These features make module operation stable at frequencies beyond 40 GHz. We also demonstrate a DC-to-40-GHz distributed amplifier IC module that uses this new technology.

Introduction

Ultra-high-speed optical transmission systems are expected to be the backbone of future multimedia communications. A few years ago, IC modules were developed, using QFP metal packages with wire bonding, that operated at 10 Gbit/s[1]. Now there is a great need for even higher bit rates around 40-Gbit/s. But to attain this level, many technical problems must be overcome. For example, as the bandwidth is widening and the frequency is rising, the wavelength of the electrical signal is approaching the physical size of the IC and their module component such as package cavity, input / output leads, and bonding wires. We have previously proposed a "chip size cavity package" concept that can suppress the cavity resonance in packages[2]. In addition to this technique, we now introduce two more techniques. The first uses flip-chip technology to reduce reactance with bonding. The second employs FD-TD[3] and FEM field simulation to module design to deal with three dimensional structure effect of module components. We also took into account reproducibility and thermal properties. We apply the new module structure and design approaches to analog and digital IC modules and their multi-chip systems.

Module Structure Overview

Figure 1 shows our new module structure for an analog IC with two RF ports. The module comprises a metal package, a thin-film multilayer (TFM) interconnection substrate, two metal lids, and a seal cover. Using metal lids minimizes the size of the module cavity to almost that of the IC chip, to prevent cavity resonance. IC chips are mounted face down to the TFM substrate by means of bumps.

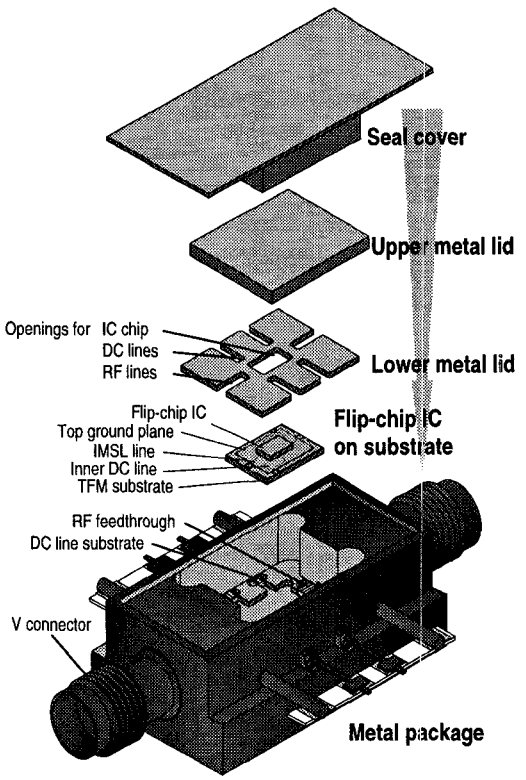

Figure 1: A view of two-port-RF analog module

Figure 2 is a photograph of our new modules for analog and digital ICs, which measure 13 × 20 × 11 and 21 × 25 × 11 mm, respectively. In addition to excellent electrical performance, these modules can be hermetically sealed, including their RF connectors. This makes it easy to package a variety of ICs by varying the design of the TFM substrate and the lower metal lid.

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Moreover, this module structure is suitable for multi-chip applications because of the interconnection capability and because the electromagnetic fields of individual IC chips are highly isolated by the chip-size-cavity structure.

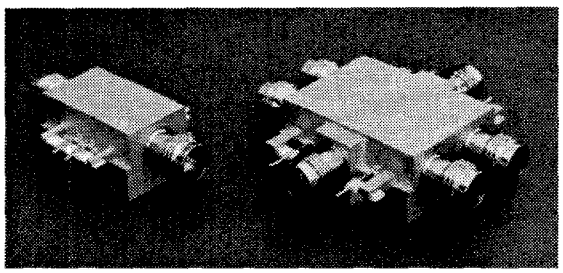

Figure 2: Photograph of modules.

TFM Interconnection Substrate Structure

A schematic of the TFM substrate is shown in Figure 3. It is constructed with three polyimide multilayers on a ceramic base. Because heat dissipation is only possible via the bumps, to reduce thermal resistance the ceramic substrate is made from AlN. There is a total of four metal layers. The first, which is on the substrate surface, is used as a ground plane and is in electrical contact through embedded via holes with the metallized back of the substrate. The second layer is employed to construct DC and RF lines. Almost all of the third metal layer serves as a ground plane. Most of the top layer serves mainly as barrier metal for bumps, the rest serves as a ground plane. Because the metal lids are in electrical contact with the top metal layer ground plane, transmission lines must be constructed using an IMSL (inverted microstrip line) structure.

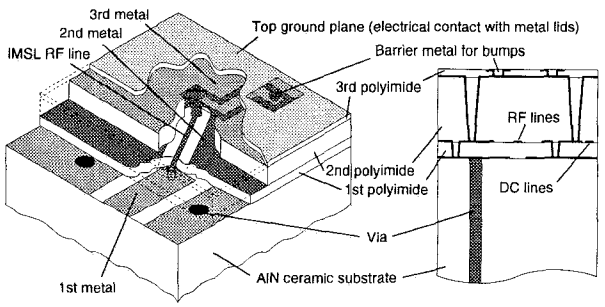

Figure 3: Views of the TFM interconnection substrate.

The experimental and simulated S-parameters of a 2-mm-long, 50-Ω IMSL is shown in Figure 4. The insertion loss is less than 0.6 dB / mm in the frequency region below 50 GHz.

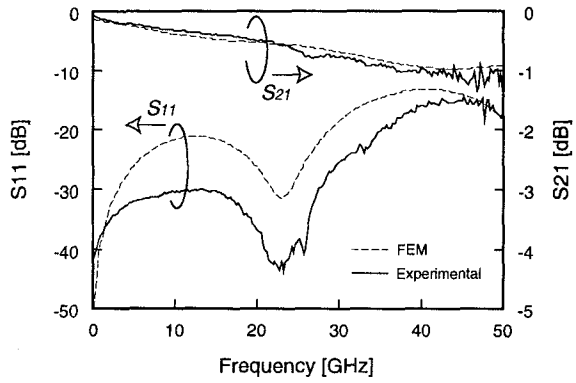

Figure 4: S-parameters of 50-Ω IMSL.

Key Technologies

In order to guarantee 40-Gbit/s module operation, our design target was to increase the bandwidth of the module to 50 GHz. At such high frequencies, because the three-dimensional distributed effects of module components must be controlled in designs, we extensively used electromagnetic field simulations to deal with that effects.

Chip Size Cavity Structure

The IC chip is shielded by two metal lids and the top ground plane of the TFM substrate. These make the cavity size almost the same as that of the IC chip. This structure puts the cavity resonance frequency outside of the module bandwidth. To suppress dielectric coupling, the IC chip and the DC and RF lines are electromagnetically isolated by lids and package metal blocks. The isolation characteristics of the new module structure are shown in Figure 5. The isolation is significantly improved with lids, less than -60 dB below 50 GHz, compared to that without lids.

Feedthrough Design

The feedthroughs are constructed of CPW line fabricated on alumina substrate and are shielded by metal lids and package metal blocks. As the frequency becomes higher, excitation of rectangular waveguide modes cannot be ignored in this type of grounded CPW structure. The feedthrough structure was designed using FEM field

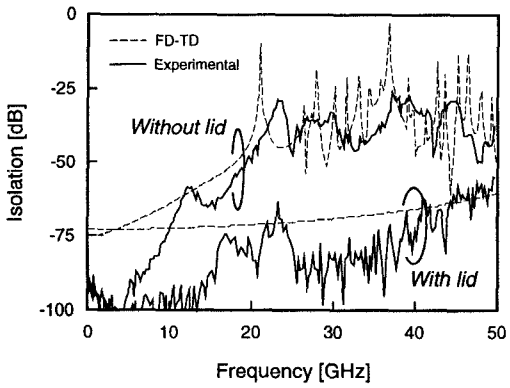

Figure 5: Isolation characteristics of new module structure.

simulation to attain the lowest cutoff frequency outside the bandwidth. Figure 6 shows the return loss versus the feedthrough width. We designed the width to be 1 mm to keep the return loss below -20 dB up to 60 GHz. The feedthroughs are connected to the TFM substrate with bonding ribbons. The length of the ribbons is as short as possible to minimize parasitic inductance. Simulated S-parameters of the feedthrough including ribbons are shown in Figure 7. Return loss of the feedthrough is below -20 dB at frequencies up to 50 GHz.

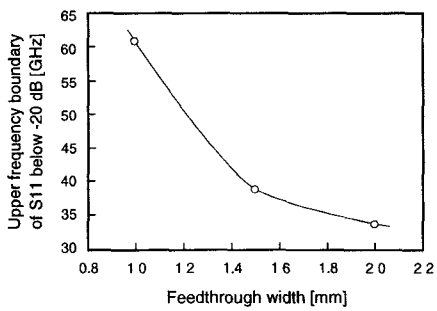

Figure 6: Feedthrough return loss versus width.

Flip-Chip Technology

Use of flip-chip bonding technology is the most efficient approach for reducing parasitic reactance at the connection between the chips and the substrates. Figure 8 shows simulated return loss of the bump bonding region at 50 GHz in relation to the bump height. We chose a height of 40 μm for the bump, to bring the return loss below -20-dB for frequencies below 50 GHz.

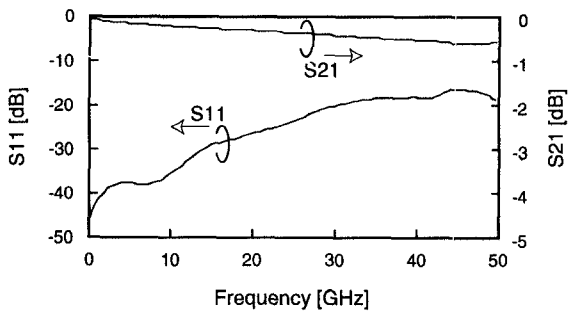

Figure 7: Simulated S-parameters of feedthrough.

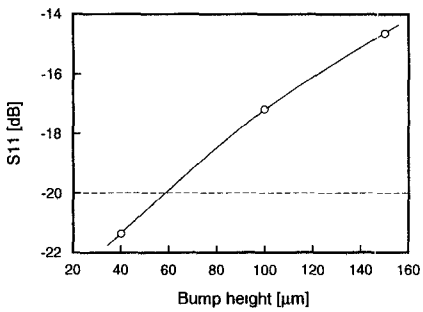

Figure 8: Simulated return loss of bump bonding region.

Module Performance

We verified the performance of the new module structure by fabricating a distributed amplifier IC module using 40 μm height solder bumps[4]. Amplifier ICs were fabricated using GaAs MESFETs with gate-length of 0.2 μm and CPW lines. The distributed amplifier was designed especially for optical communication applications and used a new circuit that extended the lowest frequency limit of flat gain to kilohertz frequencies[5]. The IC dissipates 1.1W of power. The frequency dependencies of the S-parameters for the module are shown in Figure 9. The module had a low frequency gain of 7 dB and a 3-dB bandwidth of 40 GHz. S11 and S22 were below -10 dB at frequencies below 40 GHz. Figure 10 shows 40-Gbit/s input and output waveforms of the amplifier module. The input eye pattern was generated by a InAlAs/InGaAs/InP HEMT selector module[6]. This selector module had the same structure as the one reported here except that it used ribbon bonding for connections between the chip and the substrate because the clock frequency of this module was

20 GHz. The output eye pattern showed a little distortion but clear eye opening was confirmed.

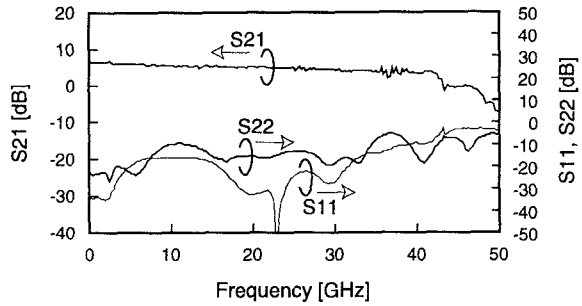

Figure 9: S-parameters of the amplifier module.

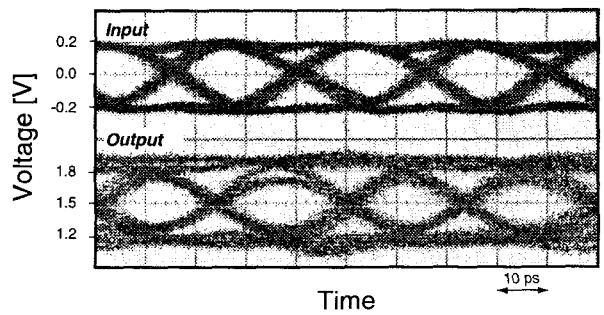

Figure 10: Waveforms of the amplifier module.

Figure 11 shows the thermal image of the amplifier IC channel flip-chip mounted in the module measured by IR scan technique. The numbers in this figure indicate the temperature differences between the IC channel and the module bottom. A maximum temperature difference of 30 degree is low enough for stable operation and module reliability.

Conclusion

We have proposed a new module structure and design approaches for ultra-high-speed optical communication ICs and confirmed its validity through a demonstration of the performance of a 40-GHz distributed amplifier module. We also measured the thermal properties of the amplifier module and confirmed their good thermal characteristics.

Acknowledgments

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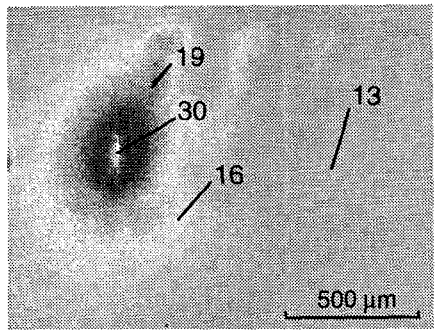

Figure 11: Thermal image of flip-chip mounted IC.

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